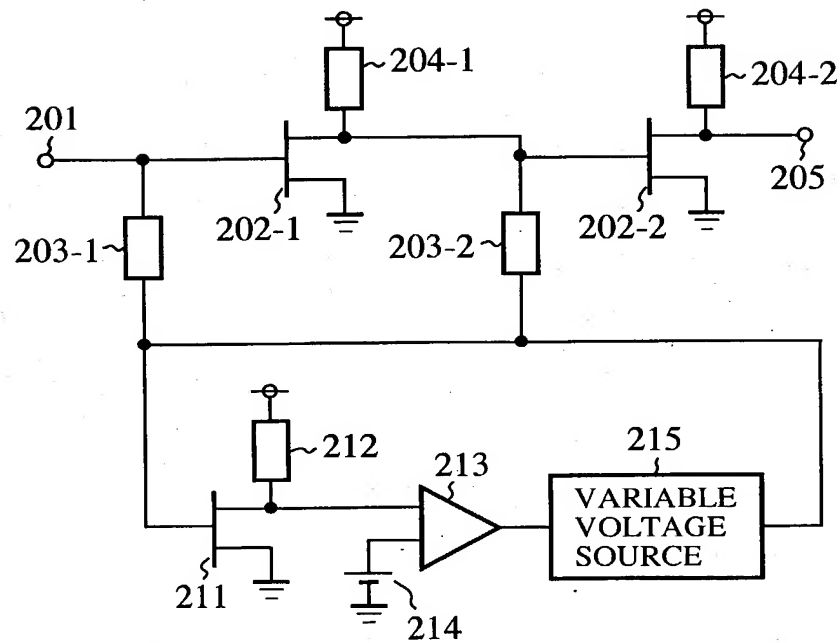
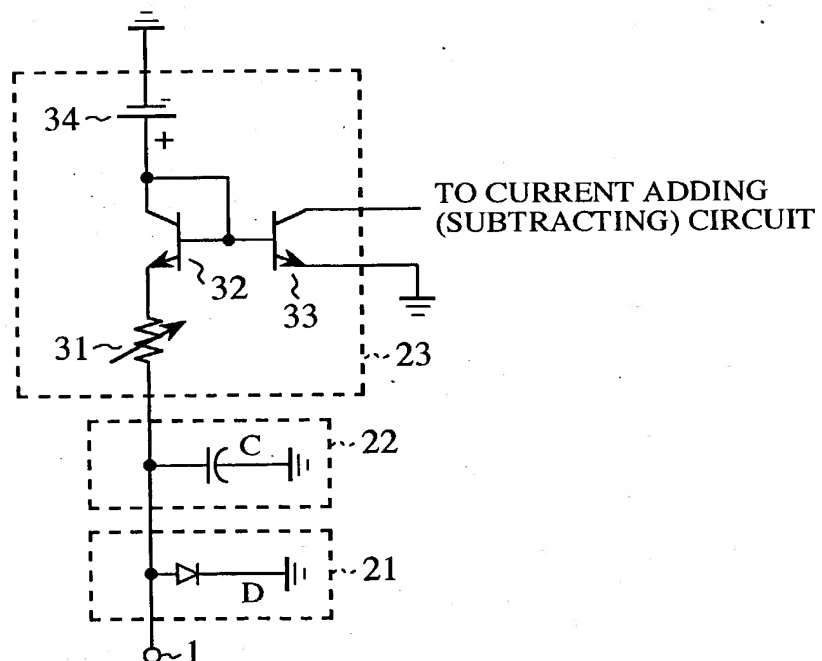


FIG.1



**FIG.3**



The diagram illustrates a multi-channel signal processing circuit. It is organized into three main functional blocks:

- Detector and Smoothing Section (21, 22):** This block receives input 1 and produces output 27. It contains a **DETECTOR CIRCUIT** (21) and a **SMOOTHING CIRCUIT** (22).
- Bias and Current Adjustment Section (23, 24, 25):** This block receives input 26 and produces output 27. It contains a **BIAS APPLYING CIRCUIT** (25), a **CURRENT ADDING CIRCUIT** (24), and a **DETECTION ADJUSTING CIRCUIT** (23).
- Multi-Channel Amplifier Section (2):** This section consists of  $N$  parallel channels. Each channel includes:
  - A **DETECTOR** (11-1 to 11-N) connected to input 1.
  - A **CURRENT SOURCE** (12-1 to 12-N) connected to the detector output.
  - A **FEEDBACK RESISTOR** (13-1 to 13-N) connected to the current source output and the detector input.

The overall output of the circuit is 3.

FIG.4

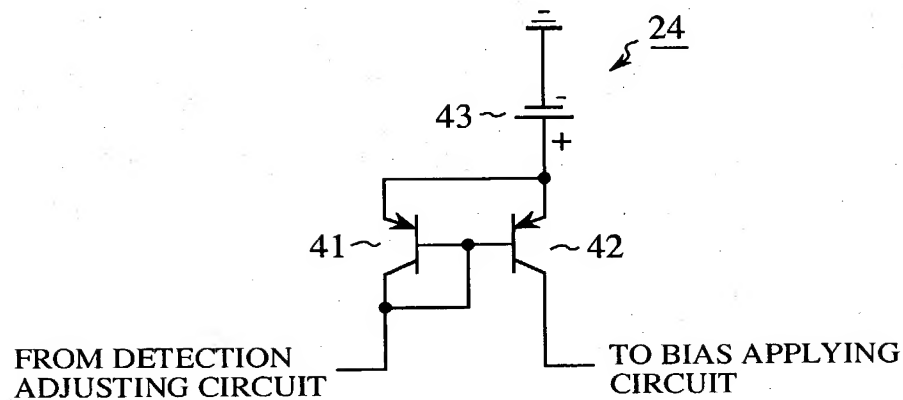


FIG.5

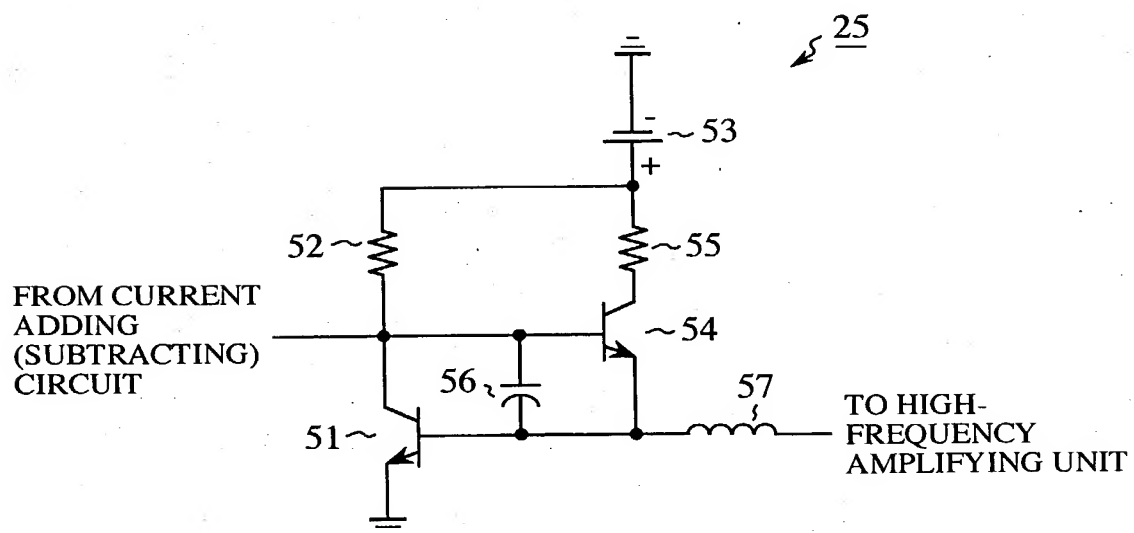


FIG. 6

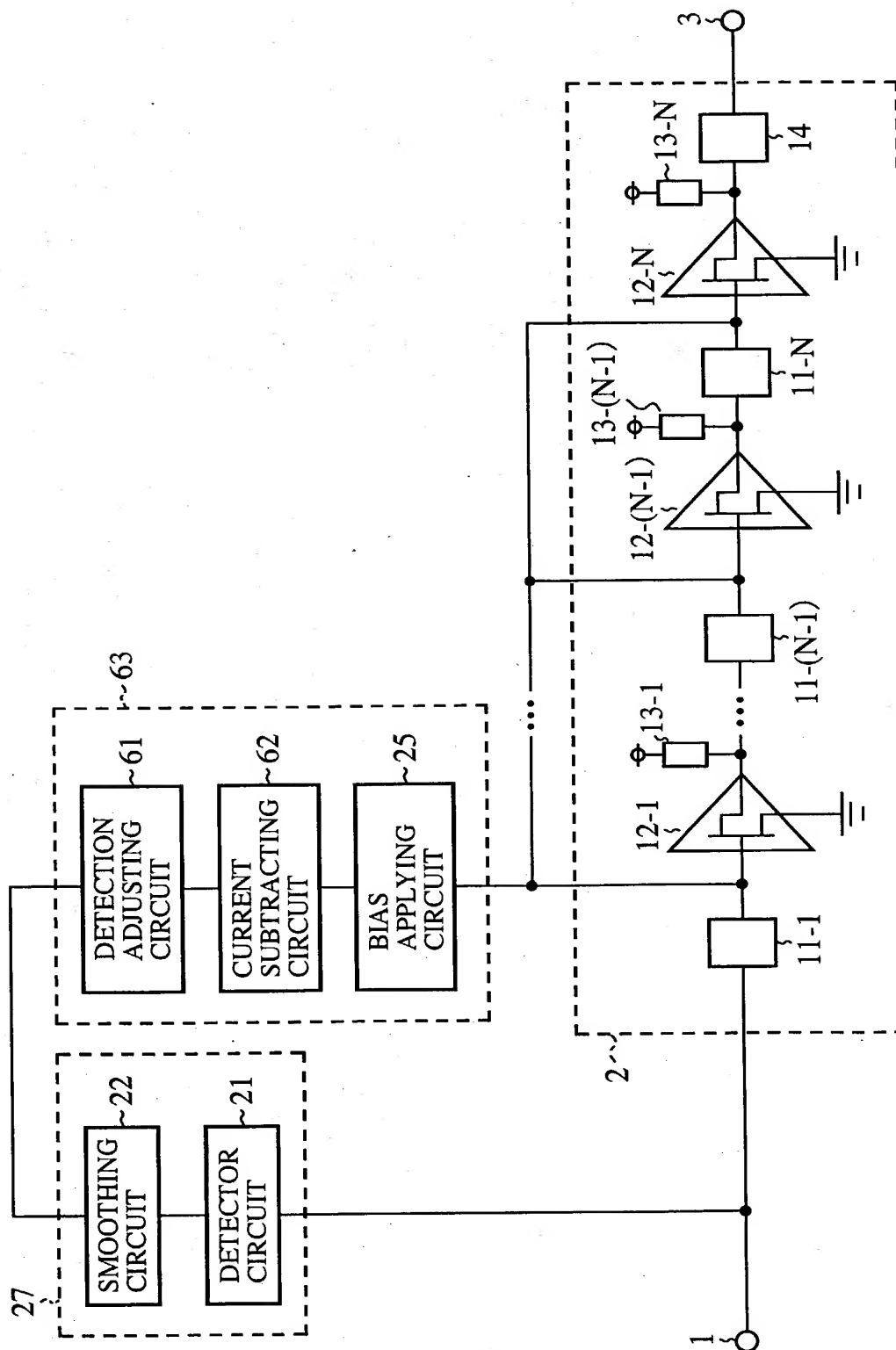


FIG.7

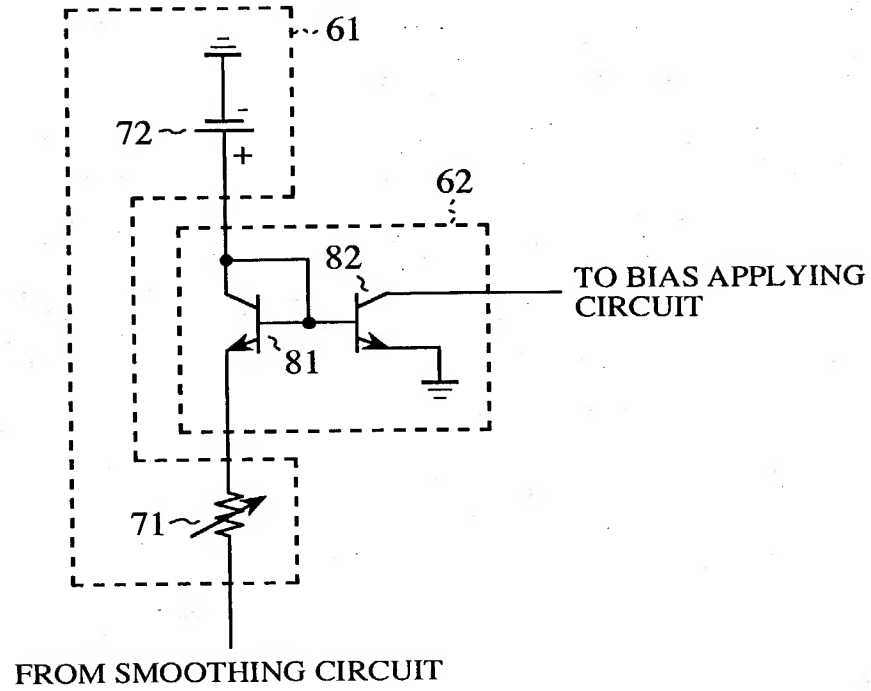
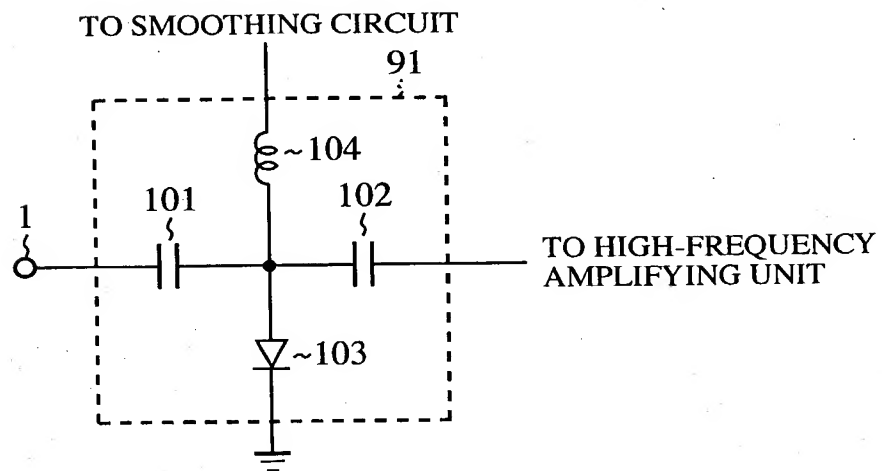


FIG.12



The diagram illustrates a multi-channel signal processing system. A dashed box labeled 27 encloses a 'SMOOTHING CIRCUIT' 22 and a 'DETECTOR CIRCUIT' 21. The output of the detector circuit is connected to a common line 1. This line branches into multiple channels, each containing a 'BIAS CONTROL CIRCUIT' 26. The outputs of these circuits are connected to a series of comparators (12-1, 12-(N-1), 12-N) and logic blocks (11-1, 11-(N-1), 11-N). The final outputs are labeled 14, 13-1, 13-(N-1), and 13-N.

7/9

FIG. 9

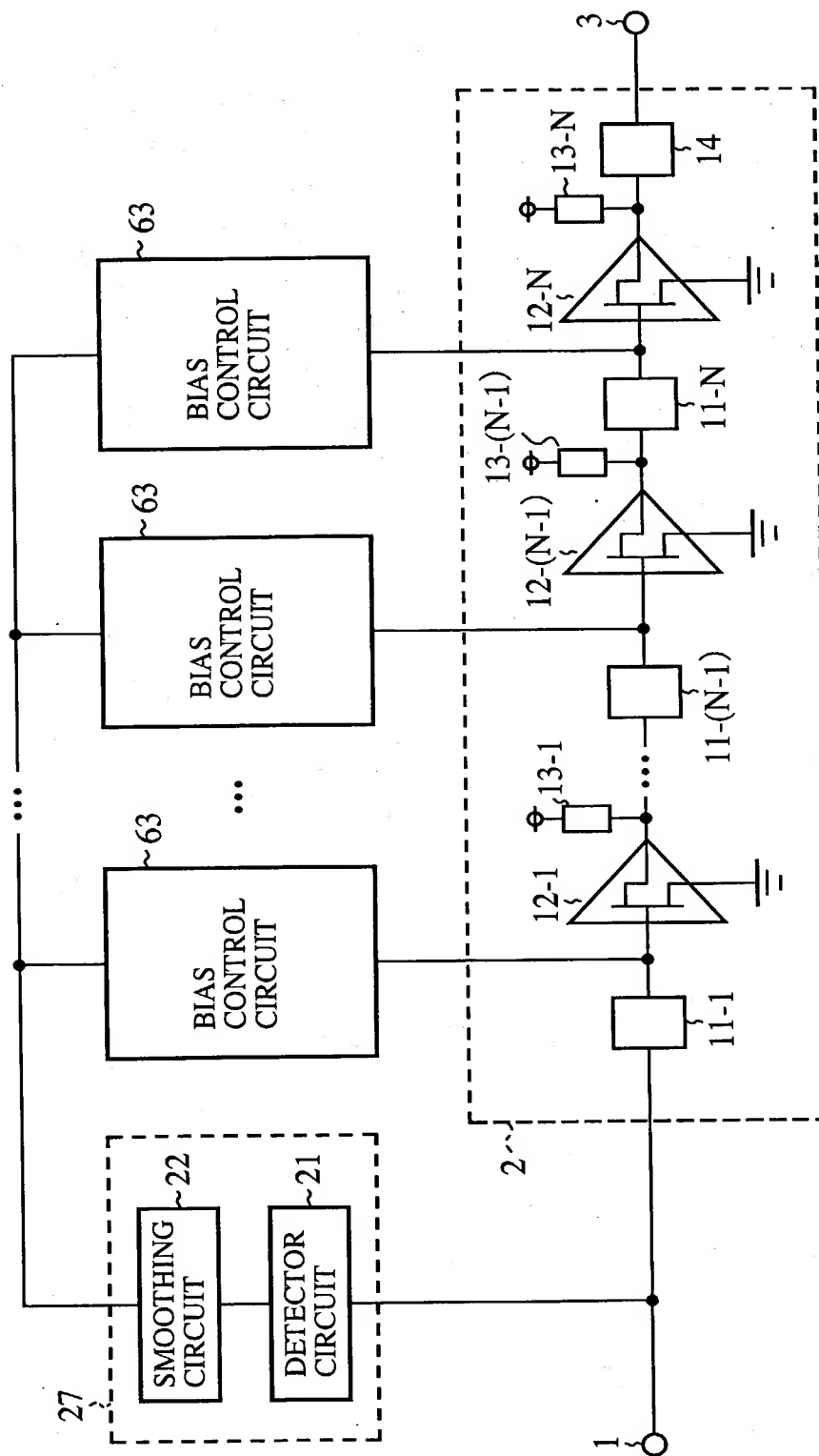


FIG.10

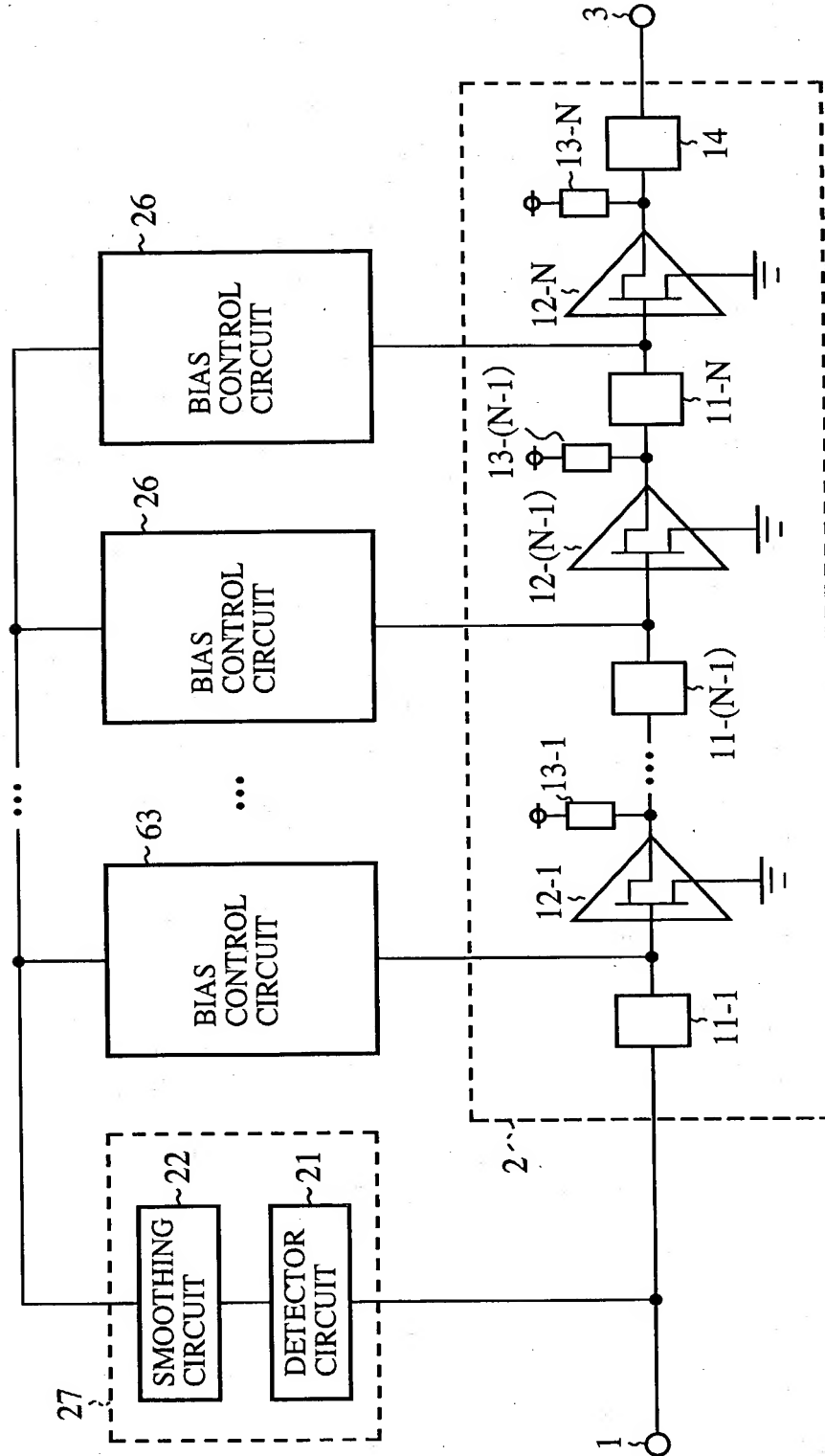




FIG. 11

